DDR SDRAM Unbuffered MODULE

184pin Unbuffered Module based on 32Mbx8 & 64Mbx8

64/72-bit Non-ECC/ECC

512MB Unbuffered DIMM DDR SDRAM

1.0 Feature

- V_{DD}: 2.5V ± 0.2V, V_{DDQ}: 2.5V ± 0.2V for DDR333
- V_{DD}: 2.6V ± 0.1V, V_{DDQ}: 2.6V ± 0.2V for DDR400
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQ] x8)
- Differential clock inputs(CK and $\overline{CK}$)
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency : DDR333(2.5 Clock), DDR400(3 Clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1,250 (mil) & single (512MB), double (512MB) sided
- SSTL_2 Interface
- 66pin TSOP II package

2.0 Ordering Information

Part number	Density	Organization	Component composition	No. of rank	Height
			x64 Non ECC		
D32PB12C25	512MB	64x64	32mx8 TSOP II	2	1.25”
D32PA512N	512MB	64x64	64Mx8 TSOP II	1	1.25”
			x72 ECC		
	512MB	64x72	32mx8 TSOP II	2	
	512MB	64x72	64Mx8 TSOP II	1	

3.0 Operating Frequencies

	CC(DDR400@CL=3)	B3(DDR333@CL=2.5)
Speed @CL2		133MHz
Speed @CL2.5	166MHz	166MHz
Speed @CL3	200Mhz	
CL-tRCD-tRP	3-3-3	2.5-3-3

4.0 Absolute Maximum DC Rating

Symbol	Parameter	Rating	Units
$V_{in,}$ Vout	Voltage on any pin relative to V_{SS}	-0.5 ~ 3.6	V
V_{DD}, V_{DDQ}	Voltage on V_{DD} & Vddq supply relative to Vss	-1.0 ~ 3.6	V
Ios	Short circuit current	50	mA
Pd	Power dissipation	1.5 * #of component	w
T_{STG}	Storage Temperature	55 ~ + 150	°C

Note:

- Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
- Functional operation should be restricted to recommended operating condition.
- Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

5.0 DIMM Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	$\overline{RAS}$
2	DQ0	33	DQ24	63	$\overline{WE}$	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	CAS	96	VDDQ	127	DQ29	157	$\overline{CS0}$
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	*CS2	102	NC	133	DQ31	163	*CS3
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	CK2	106	DQ13	137	$\overline{CK0}$	167	*A13
15	VDDQ	46	VDD	76	$\overline{CK2}$	107	DM1	138	$\overline{CK0}$	168	VDD
16	$\overline{CK1}$	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

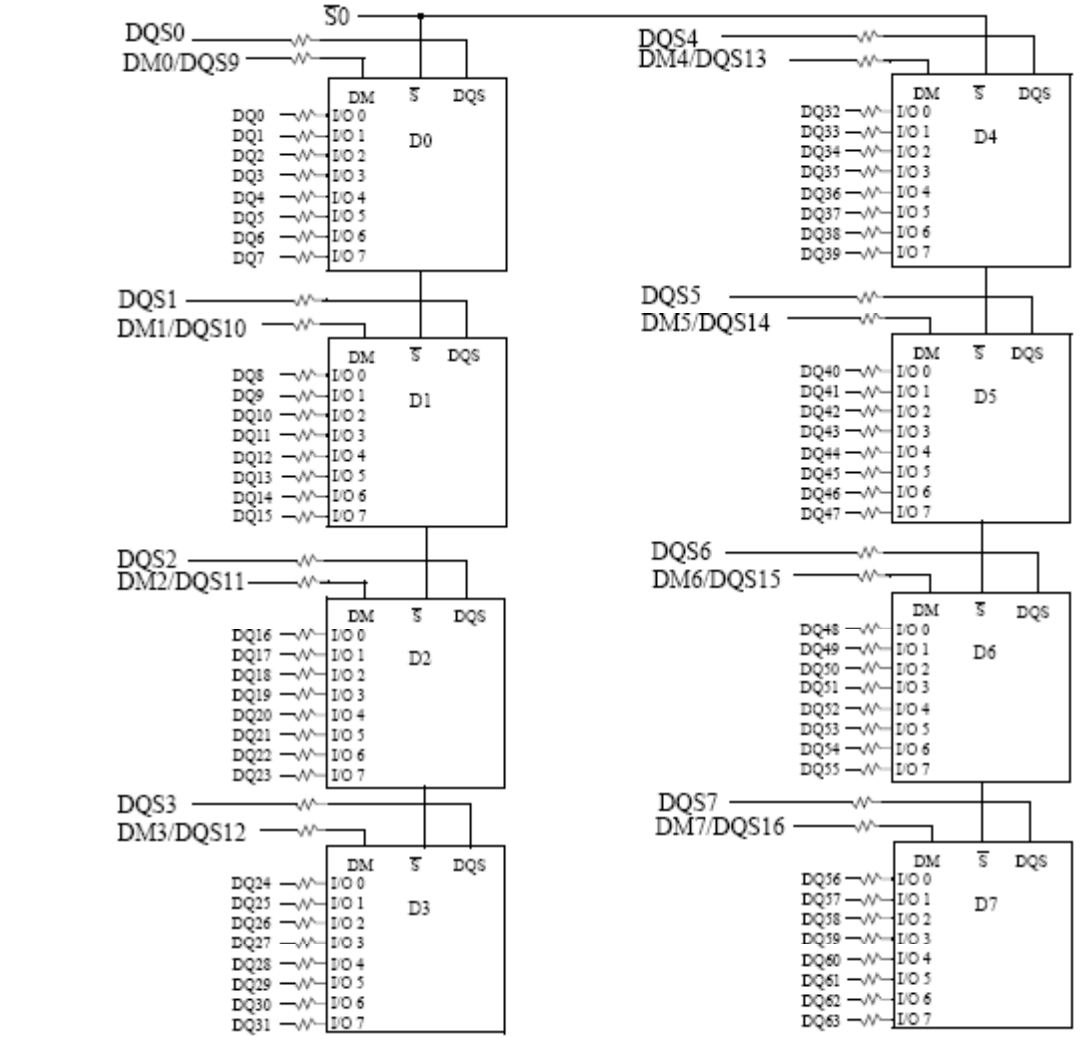
Note: * These pins are not use in this module

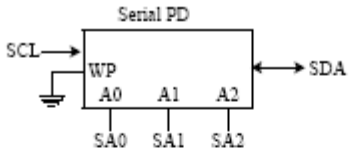
6.0 Dimm Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (multiplex)	DM0 ~ DM7	Data in mask
BA0 ~ BA1	Bank Select Address	VDD	Power Supply (2.5V for DDR333, 2.6V FOR DDR400)
DQ0~DQ63	Data input/output	VDDQ	Power Supply for DQS (2.5V for DDR333, 2.6V for DDR400)
DQS0~DQS7	Data Strobe input/output	VSS	Ground
CK0, CK0 ~ CK2, CK2	Clock input	VREF	Power Supply for reference
CKE0, CKE1	Clock enable input	VDDSPD	Serial EEPROM Power/Supply (2.3V to 3.6V)
CS0, CS1	Chip select input	SDA	Serial data I/O
RAS	Row address strobe	SCL	Serial clock
CAS	Column address strobe	SA0~2	Address in Eeprom
WE	Write enable	VDDID	VDD, VDDQ level detection

7.0 Functional Block Diagram:

7.1 512MB, 64x64 Module (populated as 1 rank of 64x8 SDRAMs)

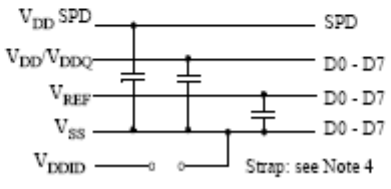




* Clock Wiring	
Clock Input	SDRAMs
*CK0/$\overline{CK0}$	2 SDRAMs
*CK1/$\overline{CK1}$	3 SDRAMs
*CK2/$\overline{CK2}$	3 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

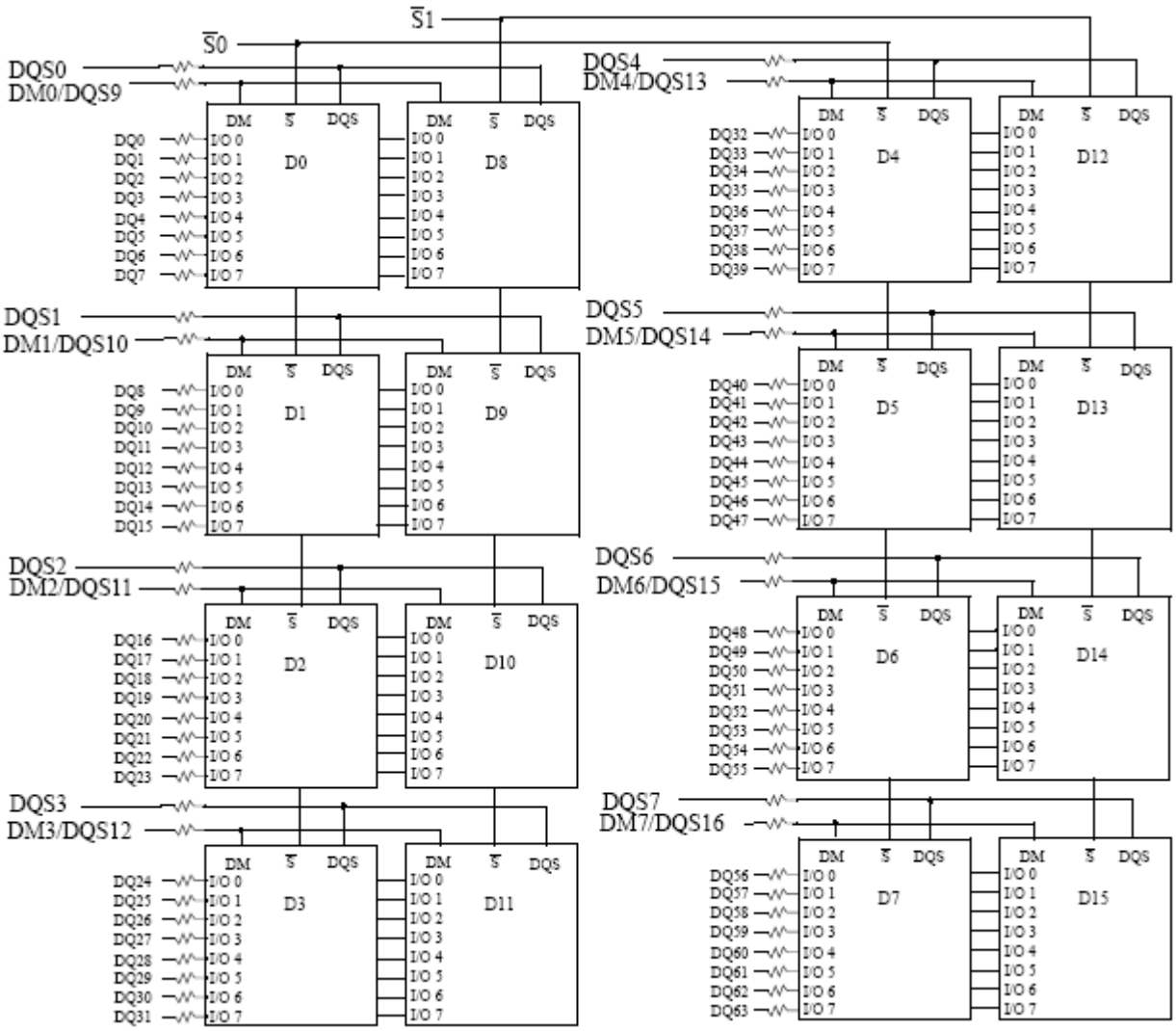
BA0 - BA1 → BA0-BA1: SDRAMs D0 - D7
A0 - A13 → A0-A13: SDRAMs D0 - D7
$\overline{RAS}$ → $\overline{RAS}$: SDRAMs D0 - D7
$\overline{CAS}$ → $\overline{CAS}$: SDRAMs D0 - D7
CKE0 → CKE: SDRAMs D0 - D7
$\overline{WE}$ → $\overline{WE}$: SDRAMs D0 - D7

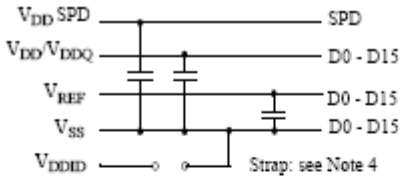


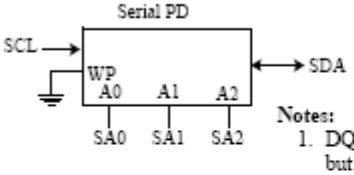
Notes:

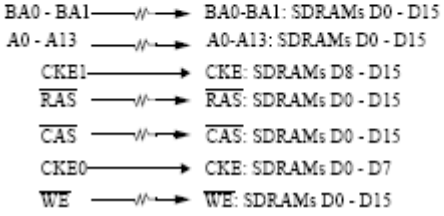
1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 5.1 ohms ±5%

7.2 512MB, 8x64 Module (populated as 2 rank of 32x8 SDRAMs)









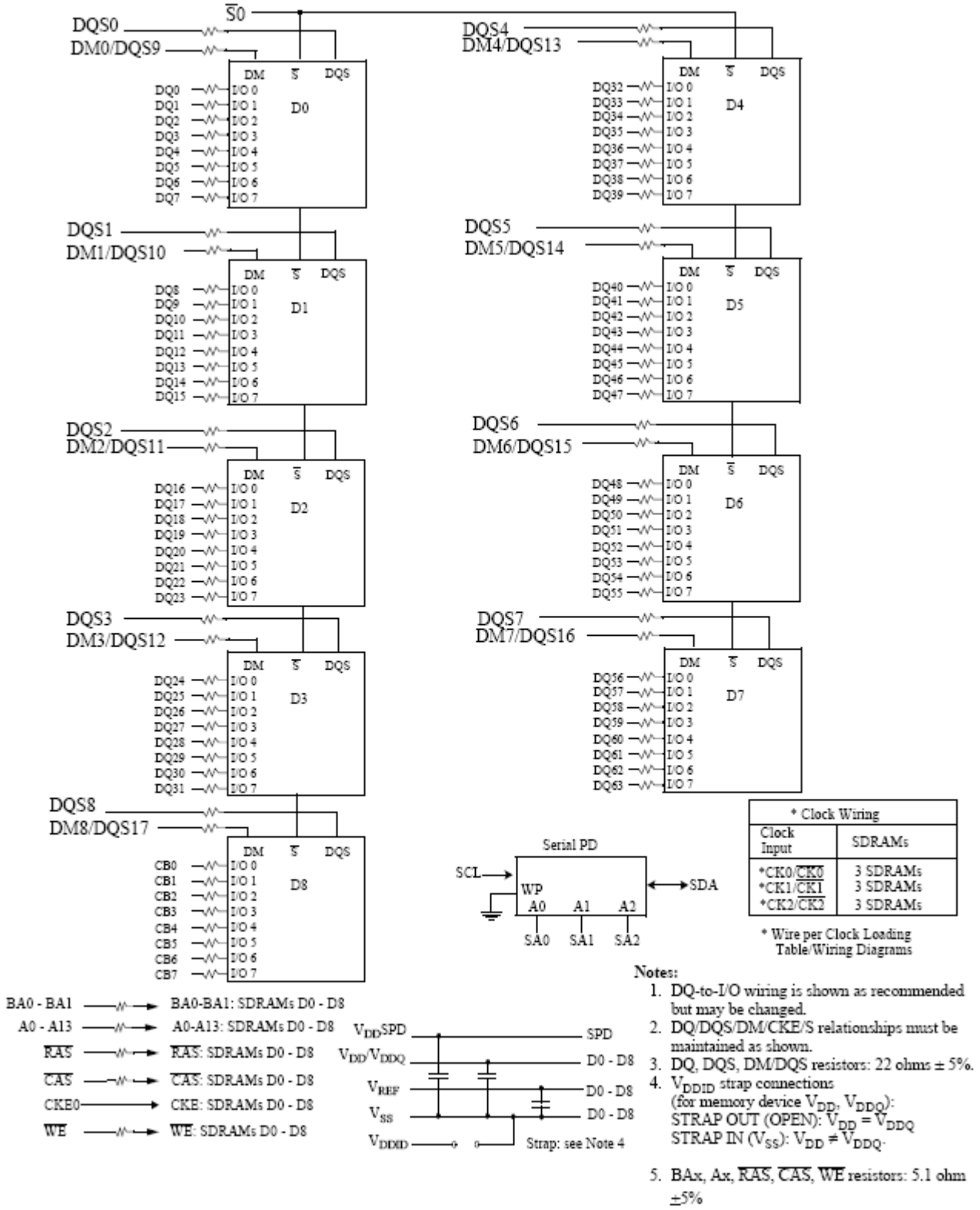
* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	4 SDRAMs
*CK1/CK1	6 SDRAMs
*CK2/CK2	6 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections
   (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$
5. BAx, Ax, RAS, CAS, WE resistors: 3 ohms ±5%

7.3 512MB, 64mx72 Module (populated as 1 rank of 64x8 SDRAMs)



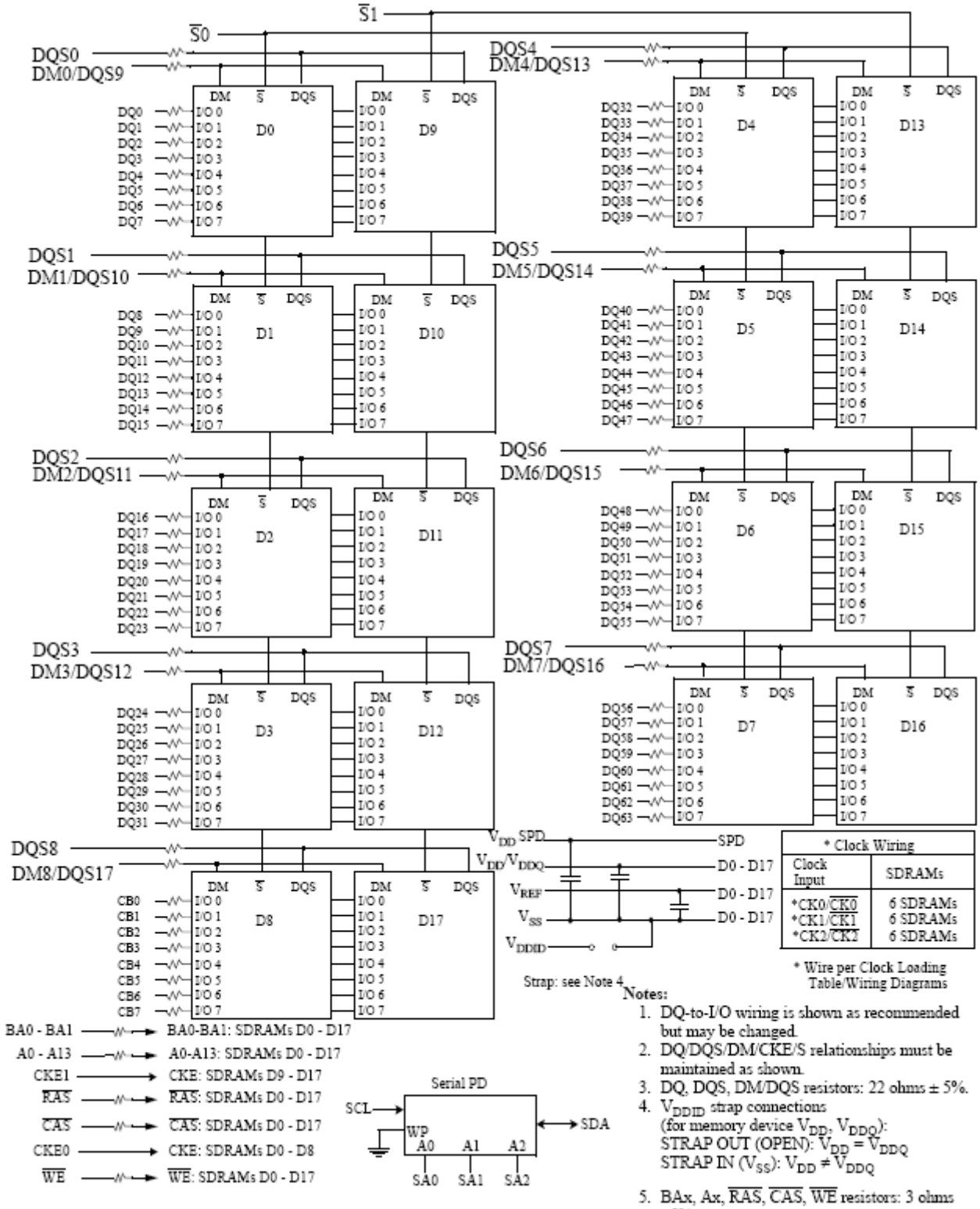
* Clock Wiring	
Clock Input	SDRAMs
*CK0/CK0	3 SDRAMs
*CK1/CK1	3 SDRAMs
*CK2/CK2	3 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}): STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$ STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. BAx, Ax, RAS, CAS, WE resistors: 5.1 ohm ±5%

7.4 512MB, 64x72 Module (populated as 2 rank of 32x8 SDRAMs)



Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 ohms ± 5%.
4. V_{DDID} strap connections
   (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$
5. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors: 3 ohms ±5%

8.0 DC Operating Conditions

Recommended operating conditions (Voltage referenced to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Max	Unit	Note
V_{DD}	Supply voltage (nominal Vdd 2.5V for DDR333)	2.3	2.7	V	
V_{DD}	Supply voltage (nominal VDD 2.6V for DDR400)	2.5	2.7	V	
V_{DDQ}	Supply voltage (nominal Vdd 2.5V for DDR333)	2.3	2.7	V	
V_{DDQ}	Supply voltage (nominal VDD 2.6V for DDR400)	2.5	2.7	V	
V_{REF}	I/O Reference voltage	$0.49*V_{DDQ}$	$0.51*V_{DDQ}$	V	
V_{TT}	I/O Termination voltage (system)	V_{REF}-0.04	V_{REF}+0.04	V	
V_{IH}(DC)	Input logic high voltage	V_{REF}+0.15	V_{DDQ}+0.3	V	
V_{IL}(DC)	Input logic low voltage	-0.3	V_{REF}-0.15	V	
V_{IN}(DC)	Input voltage level, CK and CK inputs	-0.3	V_{DDQ}+0.3	V	
V_{ID}(DC)	Input differential voltage, CK and CK inputs	0.36	V_{DDQ}+0.6	V	
V_I(Ratio)	V-I Matching: Pullup to Pulldown Current Ration	0.71	1.4	-	
I_{IN}	Input leake current	-2	2	µA	
I_{OZ}	Output leakage current	-5	5	µA	
I_{OH}	Output high current (Normal strengh driver); $V_{OUT} = V_{TT} + 0.84V$	-16.8		mA	
I_{OL}	Output high current (Normal strengh driver); $V_{OUT} = V_{TT} - 0.84V$	16.8		mA	
I_{OH}	Output high current (Half strengh driver); $V_{OUT} = V_{TT} + 0.45V$	-9		mA	
I_{OL}	Output high current (Half strengh driver); $V_{OUT} = V_{TT} - 0.45V$	9		mA	

9.0 AC Operating Conditions

Symbol	Parameter/Condition	Min	Max	Unit	Note
V_{IH}(AC)	Input High (Logic 1) Voltage, DQ, DQS and DM signals	V_{REF}+0.31		V	
V_{IL}(AC)	Input Low (Logic 0) Voltage, DQ, DQS and DM signals		V_{REF}+0.31	V	
V_{ID}(AC)	Input voltage level, CK and CK inputs	0.7	V_{DDQ}+0.6	V	
V_{IX}(AC)	Input crossing point voltage, CK and CK inputs	$0.5*V_{DDQ}$-0.2	$0.5*V_{DDQ}$-0.2	V	

10. Input/Output Capacitance

V_{DD}=2.5V, V_{DDQ}=2.5V, T_A=25°C, f=1MHZ

Symbol	Parameter/Condition	D32PA512N				Unit
		Min	Max	Min	Max	
C_{IN1}	Input capacitance (A0~A12, BA0~BA1, RAS, CAS, WE)	49	57	51	60	pF
C_{IN2}	Input capacitance (CKE0)	42	50	44	53	pF
C_{IN3}	Input capacitance (CS0)	42	50	44	53	pF
C_{IN4}	Input capacitance (CLK0, CLK1, CLK2)	25	30	25	30	pF
C_{IN5}	Input capacitance (DM0 ~ DM7, DM8 (for ECC))	6	7	6	7	pF
C_{OUT1}	Data & DQS input/output capacitance (DQ0 ~ DQ63)	6	7	6	7	pF
C_{OUT2}	Data input/output capacitance (CB0 ~ CB7)	-	-	6	7	PF

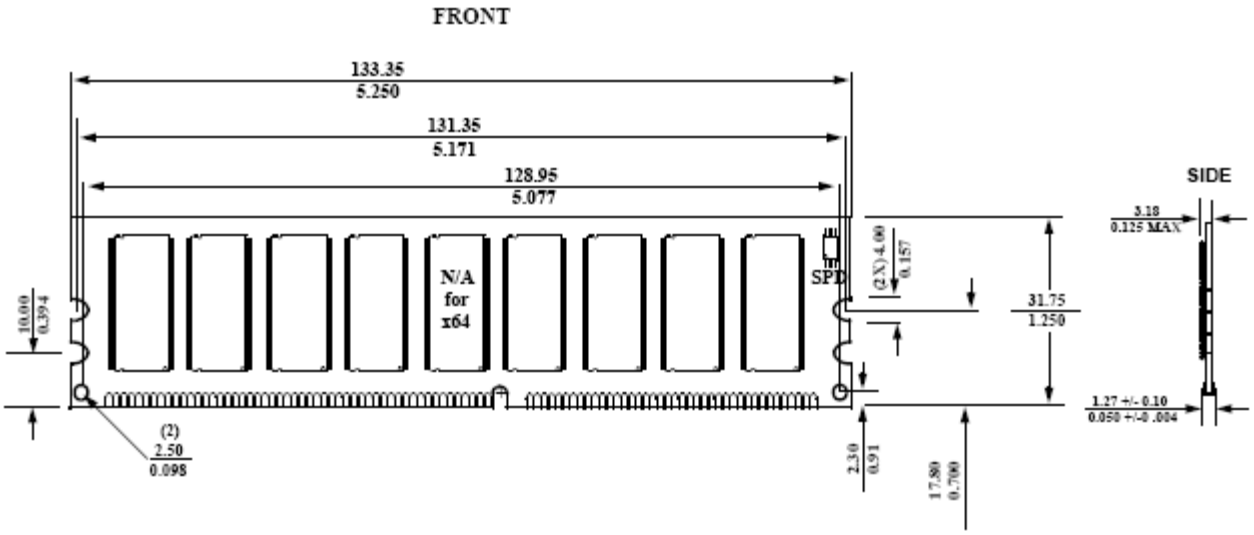
Symbol	Parameter/Condition	D32PB12C25				Unit
		Min	Max	Min	Max	
C_{IN1}	Input capacitance (A0~A12, BA0~BA1, RAS, CAS, WE)	65	81	69	87	pF
C_{IN2}	Input capacitance (CKE0)	42	50	44	53	pF
C_{IN3}	Input capacitance (CS0)	42	50	44	53	pF
C_{IN4}	Input capacitance (CLK0, CLK1, CLK2)	28	34	28	34	pF
C_{IN5}	Input capacitance (DM0 ~ DM7, DM8 (for ECC))	10	12	10	12	pF
C_{OUT1}	Data & DQS input/output capacitance (DQ0 ~ DQ63)	10	12	10	12	pF
C_{OUT2}	Data input/output capacitance (CB0 ~ CB7)	-	-	10	12	pF

11.0 AC Timing Parameters & Specifications

Parameter		Symbol	CC (DDR400@CL=3.0)		B3 (DDR333@CL=2.5)		Unit	Note
			Min	Max	Min	Max		
Row cycle time		tRC	55		60		ns	
Refresh row cycle time		tRFC	70		72		ns	
Row active time		tRAS	40	70K	42	70K	ns	
RAS to CAS delay		tRCD	15		18		ns	
Row precharge time		tRP	15		18		ns	
Row active to Row active delay		tRRD	10		12		ns	
Write recovery time		tWR	15		15		ns	
Last data in to Read command		tWTR	2		1		tCK	
Clock cycle time	CL=2.0	tCK	-	-	7.5	12	ns	
	CL=2.5		6	12	6	12	ns	
	CL=3.0		5	10	-	-		
Clock high level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQS-out access time from CK/CK		tDQSCK	-0.55	+0.55	-0.6	+0.6	ns	
Output data access time from CK/CK		tAC	-0.65	+0.65	-0.7	+0.7	ns	
Data strobe edge to output data edge		tDQSQ	-	+0.4	-	+0.45	ns	
Read Preamble		tRPRE	0.9	1.1	0.9	1.1	tCK	
Read Postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.72	1.28	0.75	1.25	tCK	
DQS-in setup time		tWPRES	0		0		ns	
DQS-in hold time		tWPRE	0.25		0.25		tCK	
DQS falling edge to CK rising-setup time		tDSS	0.2		0.2		tCK	
DQS falling edge from CK rising-setup time		tDSH	0.2		0.2		tCK	
DQS-in high level width		tDQSH	0.35		0.35		tCK	
DQS-in low level width		tDQSL	0.35		0.35		tCK	
Address and Control input setup time (fast)		tIS	0.6		0.75		ns	
Address and Control input hold time (fast)		tIH	0.6		0.75		ns	
Address and Control input setup time (slow)		tIS	0.7		0.8		ns	
Address and Control input hold time (slow)		tIH	0.7		0.8		ns	
Data-out high impedance time from CK/CK		tHZ	-0.65	+0.65	-0.7	+0.7	ns	
Data-out low impedance time from CK/CK		tLZ	-0.65	+0.65	-0.7	+0.7	ns	
Mode register set cycle time		tMRD	10		12		ns	
DQ & DM setup time to DQS		tDS	0.4		0.45		ns	
DQ & DM hold time to DQS		tDH	0.4		0.45		ns	
Control & Address input pulse width		tIPW	2.2		2.2		ns	
DQ & DM input pulse width		tDIPW	1.75		1.75		ns	
Exit self refresh to non-Read command		tXSNR	75		75		ns	
Exit self refresh to Read command		tXSRD	200		200		tCK	
Refresh interval time		tREFI		7.8		7.8	ns	
Output DQS valid window		tQH	THP-tQHS	-	THP-tQHS	-	ns	
Clock half period		tHP	TCLmin or tCHmin	-	TCLmin or tCHmin	-	ns	
Data hold skew factor		tQHS		0.5		0.55	ns	
DQS write postamble time		tWPST	0.4	0.6	0.4	0.6	tCK	
Active to Read with Auto precharge command		tRAP	15		18			
Autoprecharge write recovery + Precharged time		tDAL	(tWR/tCK) + (tRP/tCK)		(tWR/tCK) + (tRP/tCK)		tCK	

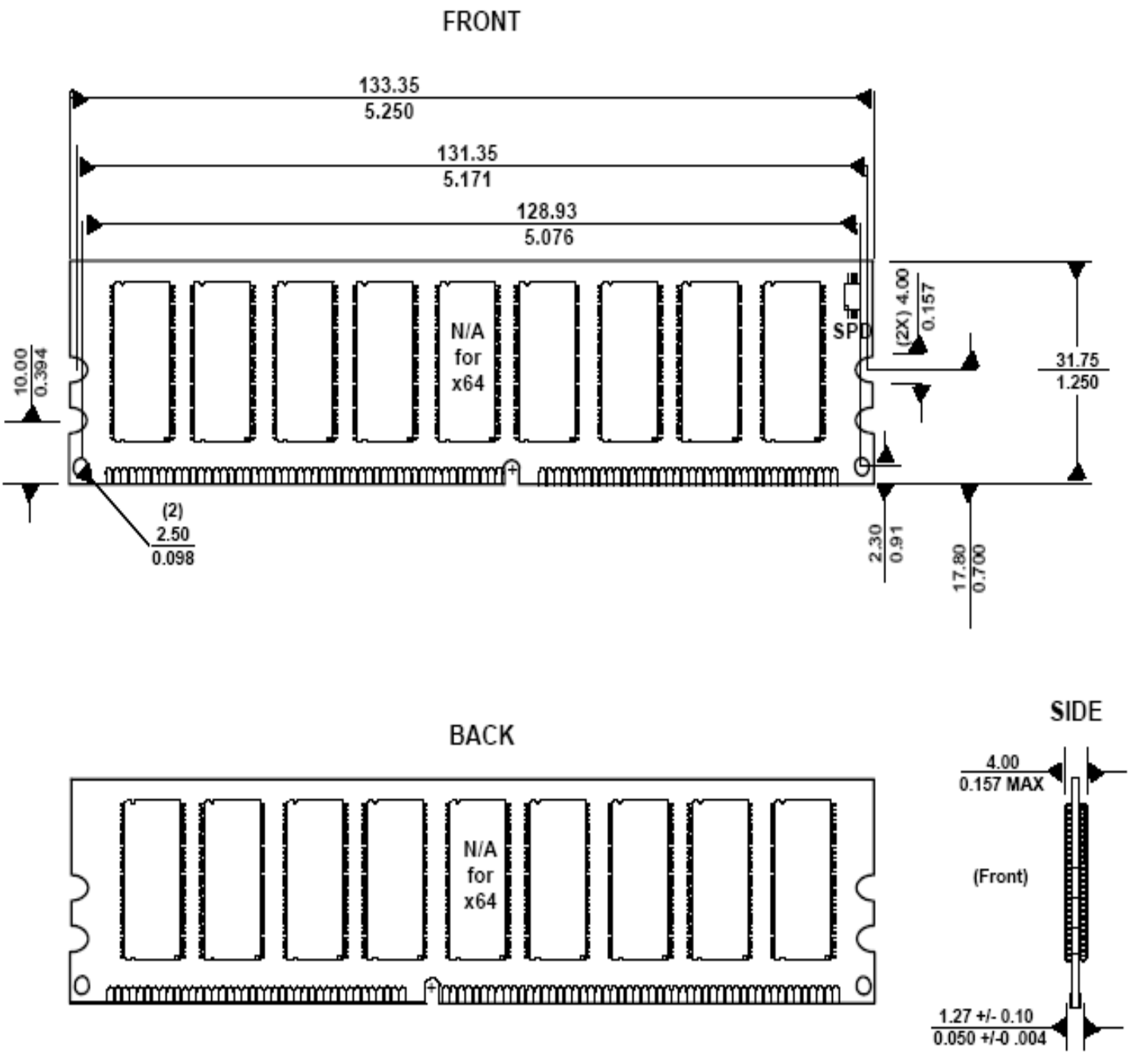
12.0 Physical Dimensions:

64Mbx8 based component, 64x64 & 64x72 Modules , populated as 1 Rank.



Note: All dimensions are typical unless otherwise state millimeters / inches

32Mbx8 based component, 64x64 & 64x72 Modules, populated as 2 Ranks



Note: All dimensions are typical unless otherwise state millimeters / inches

Revision History

Revision 1.0 (Mar. 2006)
-Initial Release